CLAIMS

What is claimed is:

1. A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests;

a read synchronization module coupled to the memory device interface, the read synchronization module operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing; and

a memory sequencer coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to adjust the timing at which read memory requests are coupled to the memory device interface responsive to the adjust signal.

2. The memory module of claim 1 wherein the link interface comprises an optical input/output port.

3. The memory module of claim 1 wherein the read synchronization module comprises a buffer coupled to at least one memory device and the memory sequencer, the buffer operable to store received read data and to subsequently output the stored read data.

4. The memory module of claim 3 wherein the read synchronization module comprises:

a write pointer coupled to at least one memory device, the write pointer operable to increment in response to read data being stored in the buffer;

a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the buffer; and

a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing.

5. The memory module of claim 1 wherein the read synchronization module comprises:

a write pointer coupled to at least one memory device, the write pointer operable to increment in response to a read strobe coupled to the memory device;

a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the memory module; and

a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing.

6. The memory module of claim 1 wherein the memory devices comprise dynamic random access memory devices.

7. The memory module of claim 1 wherein the memory sequencer is operable to increase a period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of a decrease in the timing between coupling read data from the memory devices and coupling read data from the memory hub, the memory sequencer further being operable to decrease the period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of an increase in the timing between coupling read data from the memory devices and coupling read data from the memory hub.

8. A memory module, comprising:

a plurality of memory devices, each of the memory devices being operable to output read data signals and a read data strobe signal responsive to respective memory requests; and

a memory hub, comprising:

a link interface receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple the received memory requests to at least one of the memory devices and to receive the read data signals and the read data strobe signal responsive to respective memory requests;

a buffer coupled to receive the read data signals, the read data signals being clocked into the buffer responsive to the read data strobe signal;

a read synchronization module coupled to the memory device interface, the read synchronization module operable to compare timing between the read data strobe signals and a core clock signal and to generate an adjust signal corresponding to the compared timing; and

a memory sequencer coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to adjust the timing at which read memory requests are coupled to the memory device interface responsive to the adjust signal.

9. The memory module of claim 8 wherein the link interface comprises an optical input/output port.

10. The memory module of claim 8 wherein the read data signals are clocked out of the buffer responsive to the core clock signal.

11. The memory module of claim 10 wherein the read synchronization module comprises:

a write pointer coupled to at least one memory device, the write pointer operable to increment in response to the read data strobe;

a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to the core clock signal; and

a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing.

12. The memory module of claim 8 wherein the memory devices comprise dynamic random access memory devices.

13. A memory hub, comprising:

a link interface receiving memory requests for access to memory cells in at least one memory device;

a memory device interface coupled to a plurality of memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests;

a read synchronization module coupled to the memory device interface, the read synchronization module operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing; and

a memory sequencer coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to adjust the timing at which read memory requests are coupled to the memory device interface responsive to the adjust signal.

14. The memory hub of claim 13 wherein the link interface comprises an optical input/output port.

15. The memory hub of claim 13 wherein the read synchronization module comprises a buffer coupled to at least one memory device and the memory sequencer, the buffer operable to store received read data and to subsequently output the stored read data.

16. The memory hub of claim 15 wherein the read synchronization module comprises:

a write pointer coupled to at least one memory device, the write pointer operable

to increment in response to read data being stored in the buffer;

a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the buffer; and

a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing.

17. The memory hub of claim 13 wherein the read synchronization module comprises:

a write pointer coupled to at least one memory device, the write pointer operable to increment in response to a read strobe coupled to the memory device;

a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the memory hub; and

a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing.

18. The memory hub of claim 13 wherein the memory devices comprise dynamic random access memory devices.

19. The memory hub of claim 13 wherein the memory sequencer is operable to increase a period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of a decrease in a period between the read pointer and the write pointer, the memory sequencer further being operable to decrease the period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of an increase in the period between the read pointer and the write pointer.

20. A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests;

a read synchronization module coupled to the memory device interface, the read synchronization module operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding to the compared timing; and

a memory sequencer coupled to the link interface, the memory device interface, and the read synchronization module, the memory sequencer being operable to couple memory requests to the memory device interface responsive to memory requests received from the link interface, the memory sequencer further being operable to adjust the timing at which read

memory requests are coupled to the memory device interface responsive to the adjust signal.

21. The computer system of claim 20 wherein the link interface comprises an optical input/output port.

22. The computer system of claim 20 wherein the read synchronization module comprises a buffer coupled to at least one memory device and the memory sequencer, the buffer operable to store received read data and to subsequently output the stored read data.

23. The computer system of claim 22 wherein the read synchronization module further comprises:

a write pointer coupled to at least one memory device, the write pointer operable to increment in response to read data being stored in the buffer;

a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the buffer; and

a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing.

24. The computer system of claim 20 wherein the read synchronization module further comprises:

a write pointer coupled to at least one memory device, the write pointer operable to increment in response to a read strobe coupled to the memory device;

a read pointer coupled to the memory sequencer, the read pointer operable to increment in response to read data being output from the memory module; and

a comparator coupled to the read pointer, the write pointer, and the memory sequencer, the comparator operable to compare the read pointer to the write pointer and to generate the adjust signal corresponding to the compared timing.

25. The computer system of claim 20 wherein the memory devices comprise dynamic random access memory devices.

26. The computer system of claim 20 wherein the memory sequencer is operable to increase a period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of a decrease in the timing between coupling read data from the memory devices and coupling read data from the memory hub, the memory sequencer further being operable to decrease the period between receiving the memory requests from the link interface and coupling the memory requests to the memory device interface responsive to an adjust signal indicative of an increase in the timing between coupling read data from the memory devices and coupling read data from the memory hub.

27. A method of reading data from a memory module, comprising:

receiving memory requests for access to a memory device in the memory module;

coupling the memory requests to the memory device responsive to the received memory request, at least some of the memory requests being memory requests to read data;

receiving read data responsive to the read memory requests;

outputting the read data from the memory module;

comparing timing between receiving the read data and outputting the read from the memory module; and

adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing.

28. The method of claim 27 further comprising storing the received read data in a buffer.

29. The method of claim 27 wherein the buffer comprises a circular buffer.

30. The method of claim 27 wherein the act of comparing the timing between receiving the read data and outputting the read from the memory module comprises:

incrementing a write pointer in response to receiving the read data,

incrementing a read pointer in response to outputting the read data from the memory module; and

comparing the write pointer to the read pointer.

31. The method of claim 27 wherein the act of receiving memory requests for access to a memory device mounted on the memory module comprises receiving optical signals corresponding to the memory requests.

32. The method of claim 27 wherein the act of adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing comprises:

increasing a delay between receiving the memory requests and coupling the memory requests to the memory device responsive to a decrease in the period between receiving the read data and outputting the read from the memory module, and

decreasing the delay between receiving the memory requests and coupling the memory requests to the memory device responsive to an increase in the period between receiving the read data and outputting the read from the memory module.

33. A method of coupling read data from a memory device to a buffer and outputting read data from the buffer, comprising:

coupling memory requests to the memory device, at least some of the memory requests being memory requests to read data;

receiving read data responsive to the read memory requests;

storing the received read data in the buffer;

outputting the read data from the buffer;

comparing timing between storing the read data in the buffer and outputting the read from the buffer; and

adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compared timing.

34. The method of claim 33 wherein the buffer comprises a circular buffer.

35. The method of claim 33 wherein the act of comparing the timing between storing the read data in the buffer and outputting the read from the buffer comprises:

incrementing a write pointer in response to storing the read data in the buffer;

incrementing a read pointer in response to outputting the read from the buffer; and

comparing the write pointer to the read pointer.

36. The method of claim 33 wherein the act of adjusting the timing at which read memory requests are coupled to the memory device interface comprises:

increasing a delay in coupling the memory requests to the memory device responsive to a decrease in the period between the write pointer and the read pointer, and

decreasing the delay in coupling the memory requests to the memory device responsive to an increase in the period between the write pointer and the read pointer.